بِسْمِ اللّٰهِ الرَّحْمٰنِ الرَّحِيْمِ

In the Name of Allāh, the Most Gracious, the Most Merciful

MidTerm Papers Solved MCQS with Reference (1 to 22 lectures)

1. What is the instruction length of the FALCON-A processor?
   - o 8 bits
   - o **16 bits** **PG # 91**
   - o 32 bits
   - o 64 bits
2. What is the instruction length of the SRC processor?
   - o 8 bits
   - o 16 bits
   - o **32 bits** **PG # 134**
   - o 64 bits
3. What does the word 'D' in the 'D-flip-Flop' stands for?
   - o Double
   - o **Data** **PG # 76**
   - o Digital
   - o Dynamic

4. “If P = 1, then load the contents of register R1 into register R2”. This statement can be written in RTL as:
   - o R1 ← R2
   - o P: R1 ← R2
   - o **P: R2 ← R1** Click Here For More Detail
   - o P: R2 ← R1, P: R1 ← R2
5. Almost every commercial computer has its own particular _____ language.
   - o **assembly language** **PG # 25**
   - o English language
   - o Higher level language
   - o 3GL
6. A _____ is a computer program that is used to test and debug other programs.
   - o Linker
   - o Loader
   - o **Debugger** Click Here For More Detail
   - o Compiler
7. What is the working of **Processor Status Word** (PSW)?
   - o **To hold the current status of the processor.** **PG # 28**
   - o To hold the address of the current process
   - o To hold the instruction that the computer is currently processing
   - o To hold the address of the next instruction in memory that is to be executed

8. The instruction _____ will **load** the register R3 with the contents of the memory location M [PC+56]
   - Add R3, 56
   - lar R3, 56
   - **ldr R3, 56** **PG # 47**
   - str R3, 56
9. Motorola MC68000 is an example of _____ microprocessor.
   - **CISC** **PG # 148**
   - RISC
   - SRC
   - FALCON
10. _____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
   - INC4
   - LPC
   - **PCout** **PG # 172**
   - LC
11. **Op<4..0>:= IR: <15..11>:**

    The above RTL instruction presents the _____ of the FALCON-A Instructions.
   - **operation code field** **PG # 105**
   - target register field
   - operand or address index
   - second operand

12. _____ operation is required to change the processor's state to a known, defined value.

- Change
- **Reset** **PG # 194**
- Update
- Halt

13. _____ is/are defined as the number of instructions processed per second

- **Throughput** **PG # 203**
- Latency
- Hazards
- Throughput and Latency

Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second.

14. Which of the following register(s) is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

- Instruction Register
- Memory address register
- Memory Buffer Register
- **Registers A and C** **PG # 152**

15. Anything that interrupts the normal flow of execution of instructions in the processor is called a/an _____.

- Function
- **Exception** **PG # 197**
- Assembler
- Machine

16. In pipelining _____ is increased by overlapping the instruction execution

- Latency
- **Throughput** **PG # 220**
- Execution time
- Clock speed

17. _____control signal enable the input to the PC for receiving a value that is currently on the internal processor bus.

- **LPC** **PG # 172**
- INC4
- LC
- Cout

18. In which one of the following addressing modes, data is the part of the instruction itself, and so there is no need of address calculation?

- Direct Addressing Mode
- **Immediate addressing mode** **PG # 40**
- Indirect Addressing Mode
- Register (Direct) Addressing Mode

19. Which of the following hazard occurs when attempting to access the same resource in different ways at the same time?

- RAW (read after write) data hazard
- **Structural hazard** **PG # 214**
- Branch hazard
- Complex hazard

20. _____ is the arithmetic portion of the Von Neumann architecture. It consists of registers, internal buses, arithmetic units and shifters.

- Virtual Memory
- **Data path** **PG # 151**
- Structural RTL
- Timing

21. Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?

- Arithmetic
- Control
- **Data transfer**
- Floating point

22. What functionality is performed by the instruction “lar R3, 36" of SRC?

- it will load the register R3 with the contents of the memory location M [PC+36J
- **It will load the register R3 with the relative address itself (PC+36).** **PG #48**
- It will store the register R3 contents to the memory location M [PC+36]
- No operation

23. Type A format of SRC uses _____ instructions

- **Two** **PG # 47**
- Three
- Four
- Five

24. **P: R3 ← R5**

MAR ← IR

These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

- Arrow ←
- Colon :
- **Comma ,**
- Parentheses ( )

25. FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

- 8-bits
- 24-bits
- **32-bits** **PG # 157**
- 64-bits

26. Which one of the following register holds the instruction that is being executed?

- Accumulator
- Address Mask
- **Instruction Register** **PG # 152**
- Program Counter

27. Which one of the following design levels is called the gate level?

- **Logic Design Level** **PG # 22**
- Circuit Level
- Mask Level
- Register transfer Level

28. Which one of the following is called **1-address machine**?

- **Accumulator based machines** **PG # 32**
- Stack based machines
- General purpose register machines
- CISC machines

29. For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory

- Jump
- Control
- **load/store** **PG # 89**
- Arithmetic/Logic

30. The _____ instruction is completed once memory access has been made and the memory location has been written to.

- **Store** **PG # 208**
- Branch
- Load
- Control

31. Type B format of SRC uses _____ instructions

- Two
- **Three** **PG # 47**
- Four
- Five

32. PowerPC 601 is an example of_____

- FALCON-A
- EAGLE
- **Superscalar processor** **PG # 221**
- SRC

33. Which of the following register(s) takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system?

- Instruction Register
- **Memory address register** **PG # 151**
- Memory Buffer Register
- Registers A and C

34. For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location

- DMA controllers
- Memory
- **Control signals** **PG # 171**
- Registers

35. Which of the following hazard occur when an instruction attempts to access some data value that has not yet been updated by the previous instruction?

- **Data hazard** **PG # 215**
- Structural hazard
- Branch hazard
- Complex hazard

36. Which one of the following is a bi-stable device, capable of storing one bit of information?

- Decoder
- **Flip-Flop** **PG # 76**
- Multiplexer
- Diplexer

37. _____ are faster than cache memory

- RAM
- **Registers** **PG # 33**
- Hard disk
- ROM

38. An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------

- compiler
- **cross assembler** **PG # 26**
- debugger
- linker

39. FALCON stands for _____?

- **First Architecture for Learning Computer Organization and Networks** **PG # 90**
- Final Architecture for Learning Computer Organization and Networks
- Final Analysis for Learning Computer Organization and Networks
- First Analysis for Learning Computer Organization and Networks

40. _____ is defined as the time required to process a single instruction.

- Latency & throughput
- **Latency** **PG # 203**
- Throughput
- Hazards

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